

A Fully Integrated Wireless Sensor-Brain Interface System to Restore Finger Sensation

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Abstract—This paper presents a fully integrated wireless sensor brain machine interface system to restore continuous somatosensory feedback from the hand. A wireless bi-directional neural interface system-on-chip (SoC) and a wireless sensor node design are described in this work. The neural interface integrates a 16-channel neural recording front-end, a 16-channel electrical stimulation back-end, a successive approximation analog-to-digital converter (ADC), a custom digital controller, and an ultra-wide band (UWB) wireless transceiver. The sensor node features a custom designed optical force sensor, a low-power level-crossing ADC, an UWB transmitter, and analog interface to off-chip accelerometers. The optical force sensor is developed in standard CMOS with low-cost post fabrication. Multiple sensor nodes can be used to trigger pre-defined microstimulation in different brain areas for restoring finger sensation. The prototypes have been fabricated in 180nm standard CMOS technology. Bench testing and *In-Vivo* experimental results are presented in this paper. The system was designed to investigate the first chronic interface to the cuneate nucleus of macaques, and showed a promising solution for sensation restoration in future neuroprosthetics.

Index Terms—Sensor-brain interface, bi-directional neural interface, neural recording, neural stimulation, force sensor, system-on-chip (SoC)

I. INTRODUCTION

Sensations and actions are inextricably linked. Behavioral goals are achieved by sampling the environment with the available sensory modalities and modifying actions accordingly. Somatosensory feedback is especially important to the dexterous hand movement control. Recent developments in hand prosthetics with motor pathway replacement alone do not lead to the adequate use of a paralyzed hand [1]. Artificial sensation restoration is needed for this technology to meet the performance required for clinical adoption. The sensation may be restored with direct electrical microstimulation of the brain [2]. The cuneate nucleus (CN) in the dorsal brainstem carries fine touch and proprioceptive information from the upper body, and is a suitable sensory encoding site. Besides, its compact representations may be reliably activated artificially.

Recently, our lab demonstrated the first successful chronic interface to the CN of macaques [3], which allows us to investigate the sensation encoding with CN microstimulation in freely behaving animals. Force, vibration, and motion are essential sensory information for hands. In this work, a fully integrated wireless sensor brain machine interface system is

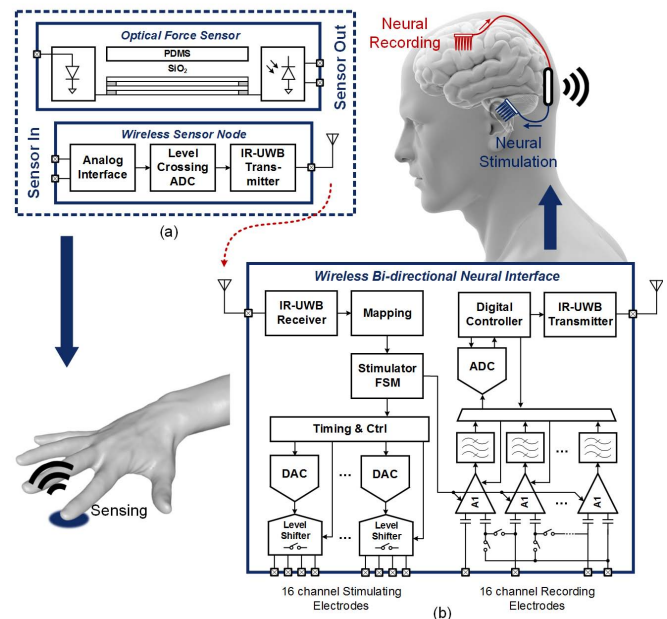


Fig. 1. The overview of the sensor brain machine interface system for restoring finger sensation through sensor controlled electrical stimulation of the brain. (a) The custom designed optical force sensor and the wireless sensor node, and (b) the bi-directional wireless neural interface SoC.

developed for finger sensation restoration. Fig. 1 illustrates the overall system, consisting of a wireless bi-directional neural interface SoC and a wireless sensor node.

This paper is organized as follows. Section II presents an overview of the system. Section III describes the circuit implementation, including the bi-directional neural interface and the wireless sensor node. The experimental results are presented in Section IV, while Section V concludes the paper.

II. SYSTEM OVERVIEW

The block diagram of the proposed fully integrated sensor brain machine interface system is shown in Fig. 1. The proposed system consists of a neural interface SoC and a sensor node. Both devices are battery powered. The neural interface integrates i) a 16-channel low noise neural recording front-end with programmable gain and bandwidth, ii) a 16-channel fully programmable electrical stimulator, iii) a 10-bit SAR ADC for neural signal digitization, iv) an IR-UWB

transceiver for wireless communication, v) digital controllers for generating timing and control signals according to received commands, and all other peripheral modules for power management and analog biasing generation. The sensor node consists of i) a custom designed optical force sensor, ii) a low-power level-crossing analog-to-digital converter (ADC), iii) a UWB transmitter, iv) analog interface to off-chip sensors, and peripheral modules. Multiple sensor nodes can be used to trigger pre-defined microstimulation in different brain areas for restoring sensation in different fingers.

III. CIRCUIT IMPLEMENTATION

A. Bi-directional Neural Interface Design

Each of the recording channel consists of a low-noise instrumentation amplifier and a programmable filter. A programmable gain amplifier and a SAR ADC is shared between the 16 channels. The circuit diagram of the low noise instrumentation amplifier is shown in Fig. 2. The main amplifier uses capacitive feedback to set the gain. The closed-loop gain is set to be 50. The main operational transconductance amplifier (OTA) A1 employs a folded-cascode topology. Chopping is optional to further remove the flicker noise in low frequency. A DC servo loop is used to set the highpass frequency and to remove the DC offset originating from the half cell potential. A capacitive positive feedback loop is used to boost the input impedance [4], especially when chopping is enabled.

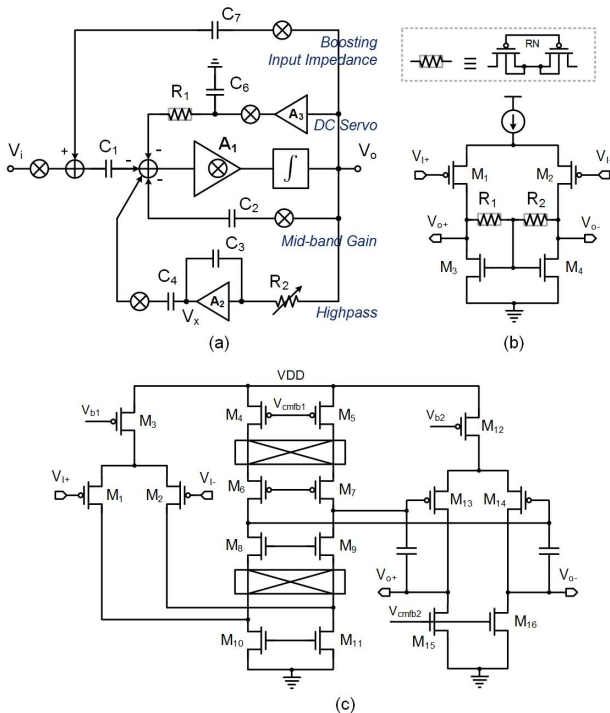


Fig. 2. (a) Block diagram of the capacitively-coupled chopping amplifier. Single-ended structure is used for illustration. (b) The circuit schematic of the fully differential amplifier used in the highpass and DC-servo loop. (c) The two stage low-noise transconductance amplifier with chopping switches.

A 16-channel multi-mode stimulator has been designed for this work. 4 channels share a driving site, which is shown in

Fig. 3. The timing of each driving site can be individually programmed, so that each site can stimulate simultaneously. Two 6-bit DACs for generating cathodic and anodic stimulation currents are merged with the output stages to minimize the power dissipation. An additional 4-bit DAC are used for calibration purposes. Regulating amplifiers are used to boost the output impedance. The stimulator module is put in the sleep mode when not in use in order to further saving power consumption.

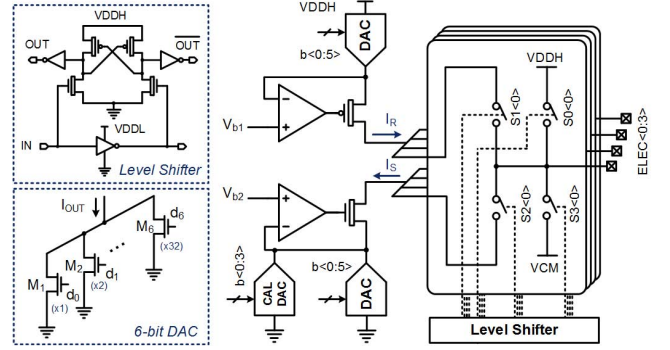


Fig. 3. The circuit schematic of the multi-mode neural stimulator.

B. Optical Force Sensor Design

The structure of the optical force sensor is shown in Fig. 4. A PDMS membrane with an inverse-lenticular structured surface is placed on top of the SiO_2 . The contact area between the PDMS and the SiO_2 is minimal when no force is applied, and the contact area increases with the force. In operation, the LED emits light into the SiO_2 optical waveguide channel. A certain amount of light internally reflects and reaches the photodiode on the other side of the waveguide. The amount of the escaped light depends on the contact area of the PDMS and the SiO_2 . Thus the readout of the photodiode changes monotonically with the applied force.

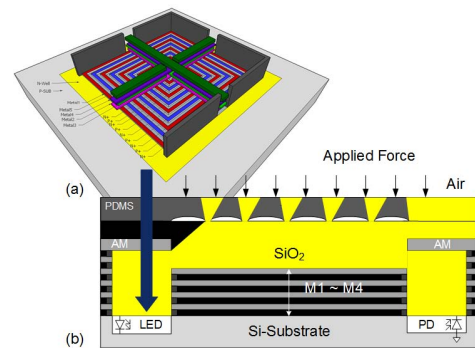


Fig. 4. (a) The 3-dimensional view of the silicon LED, which uses interdigitated P+ N+ rings inside an N-well. (b) The side view of the optical force sensor.

The PDMS material (sylgard 184 kit, Dow Corning Co.) was composed of a 1:10 mixing ratio of the curing agent. The PDMS mixture was cast on a polystyrene lenticular lens board with a pitch of $20\mu m$. After degassing for 30 minutes, the PDMS mixture and lenticular lenses molds were cured for

3 hours at 65°C. Finally, the PDMS membrane was carefully peeled off from the mold. The PDMS membrane was cut into 800 μm by 800 μm pieces and placed on top of the CMOS chip with the inverse-lenticular strips perpendicular to the direction of the optical waveguide. The thickness of the PDMS membrane is 600 μm .

The silicon LED has a size of 80 μm by 80 μm using interdigitated P+ N+ rings inside an N-well. The photodiode is also designed with a size of 80 μm by 80 μm . The readout circuit uses a 3-transistor active pixel structure. The SiO_2 optical waveguide channel has a size of 200 μm by 600 μm . The sidewalls of the LED, the photodiode and the waveguide channel are shielded by stacked metal layers and vias for minimum light leakage. The bottom side of the optical waveguide channel is elevated to metal 4 layer, which effectively prevents the light from being absorbed by the silicon substrate. It also reduces the path length of totally internally reflected light traveling inside the channel by reducing the thickness of the SiO_2 layer in the channel, which effectively reduces the light loss in the SiO_2 medium.

C. Impulse-Radio Ultra-Wide Band Wireless Transceiver

The transmitter integrates a baseband generator, an RF pulse generator, and a power amplifier. The baseband generator modulates digital input data into different numbers of short pulses. The pulse width is tunable from 10ns to 250ns under different data rates or transmission duty cycles. The RF pulse generator upconverts the short pulses to RF frequency. The oscillation frequency of the ring oscillator is tunable over a range of 100MHz. The RF pulse generator is implemented as a ring oscillator with a programmable number of stages.

In the IR-UWB receiver, the RF signal is first bandpass filtered at its corresponding operating frequency, and amplified by a low-noise amplifier. The output is fed into a radio frequency power to root-mean-square voltage (RF-RMS) converter for downconversion. A comparator recovers the baseband short pulses, and a digital pattern recognition logic circuit demodulates the recovered signal to data and clock [5].

D. Analog-to-Digital Converters

A 10-bit successive approximation register (SAR) ADC is implemented in the neural interface chip for signal digitization. A split capacitor array is used to reduce the area and power consumption. The capacitors are realized as a standard metal-insulator-metal (MIM) structure. Monotonic switching procedure is used to minimize the power consumption waste caused by unnecessary switching [6].

A 6-bit level-crossing ADC is implemented in the sensor node for low-power sensor data digitization. The level-crossing ADC tracks the changes of the input signal by comparing it with a set of hysteresis reference voltage levels using a pair of comparators. A shift register chain is used for reference voltage selection. The comparators generate output signals indicating the input voltage increases or decreases. The ADC has also been optimized for preventing self-locking states [5].

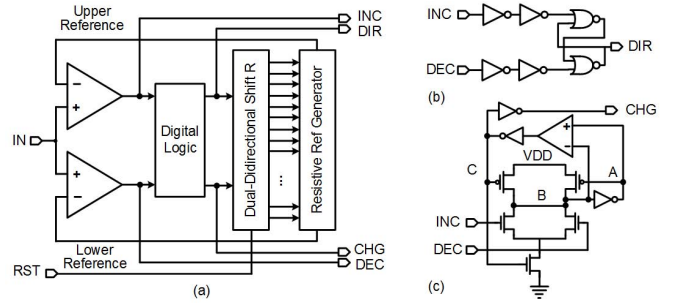


Fig. 5. (a) The block diagram for the level crossing ADC, and the circuit schematics for the (b) “change” and (c) “direction” generation modules.

IV. EXPERIMENTAL RESULTS

The designed chips have been fabricated in 180nm CMOS technology. The microphotographs of the dies are shown in Fig. 6, with major building blocks highlighted. The measured performance of the chips is listed in Table I.

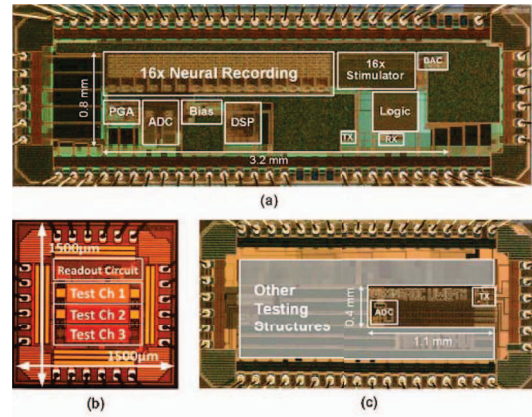


Fig. 6. The microphotography of fabricated chips in 180nm CMOS technology. (a) The bi-directional neural interface, (b) the optical force sensor, and (c) the sensor node. Major building blocks are highlighted.

TABLE I
MEASURED SPECIFICATIONS SUMMARY

| Recording Front-end | | UWB Transceiver | |
|---------------------|-------------------------------------|------------------------|-------------------------|
| LNA Gain | 34dB | TX Output power | -33dBm |
| LNA Bandwidth | 0.3Hz - 9kHz | TX/RX supply | 1.2V/0.8V |
| LNA Noise | 1.58 μV (1kHz bw) | Frequency | 1.6-1.7GHz |
| CMRR | >83dB | Max data rate | 20Mbps |
| LPF freq. | 200Hz - 6kHz | SAR/Level-crossing ADC | |
| Neural Stimulator | | Sampling Rate | 1M/5kHz |
| Stim. Current | 0 - 255 μA or 2mA | ADC ENOB | 9.1/6 |
| Amplitude Res. | 6-bit | Power supply | 1.8/0.8V |
| Pulse width | 1 μs - 250 μs | Power Consumption | |
| Stim. Frequency | 0.5Hz - 300Hz | UWB TX power | 4.6pJ/bit |
| Charge Error | 0.35 | UWB RX power | 0.32nJ/bit |
| Compliance volt | $\pm 4.9\text{V}$ | Neural Interface | 79 μW per ch |

The measured input referred noise of the neural front-end in a 0.3Hz to 1kHz bandwidth is 1.58 μV with chopping. Fig. 7 (a) shows the input referred noise spectrum with and without chopping. The frequency response of the front-end is shown in Fig. 7 (b). The mid-band gain is 49.6, and CMRR is above 83dB. The corner frequency of the low pass filter is programmable from 200Hz to 6kHz. The measured output

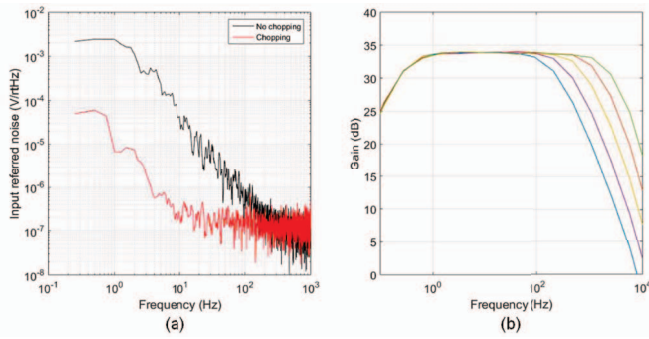


Fig. 7. Measured input referred noise of the neural amplifier with and without chopping. The rms noise from 0.3Hz to 1kHz is $1.58\mu\text{V}$.

current of the stimulator versus output voltage is shown in Fig. 8 (a). Simultaneous output of four independent channels are shown in Fig. 8 (b).

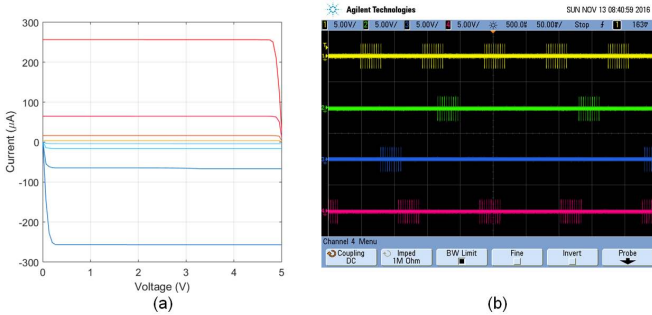


Fig. 8. The measured (a) stimulator output current vs. output voltage, and (b) independent stimulation in four channels.

Fig. 9 (a) shows the measured photodiode's output. The photodiode receives a similar amount of light with or without the PDMS membrane. With the external force applied, amount of light received by the photodiode reduces as is expected. Fig. 9 (b) shows the response of the sensor with applied force ranging from 0 to 0.87N before calibration. The response is monotonic and a lookup table (LUT) can be employed to further improve the linearity. Given the level crossing ADC is designed with 6 bits, the sensitivity of the sensor is 13.6mN.

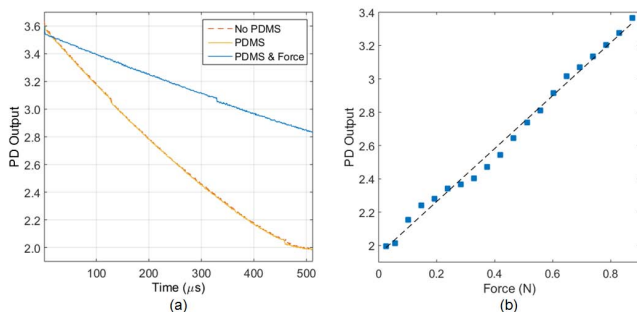


Fig. 9. Measured sensor response. (a) Photodiode output versus exposure time. The photodiode receives much less light when force is applied on the PDMS membrane sample. (b) Photodiode output with respect to the applied force. Markers are the measured data points without any calibration.

The developed system has also been tested *in-vivo*. Electrodes were implanted chronically in the left hippocampus of

a male rhesus macaque. An 8-h continuous recording while the animal was freely behaving in the home cage is shown in Fig. 10. A bi-directional *in-vivo* experiment was performed

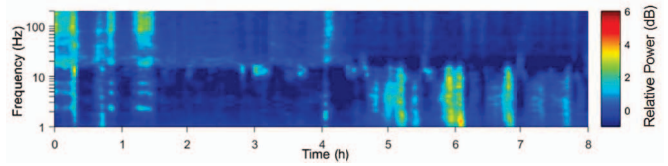


Fig. 10. The spectrum of 8 hour continuous recording using the designed neural interface. The transition between awake and sleep states can be seen from the recording.

in a female Long-Evans rat. A single pulse stimulation was repeated in the sensory cortex, and the evoked potential was recorded in the motor cortex. An overlay of the evoked potential was shown in Fig. 11 (b).

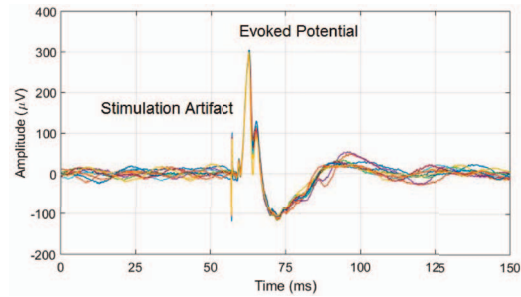


Fig. 11. In-vivo bidirectional experiment. An overlay of 10 trails of stimulation triggered evoked potential.

V. CONCLUSION

In this work, a fully integrated wireless sensor-brain machine interface system has been developed. The system includes a wireless bi-directional neural interface and a custom designed sensor node. A novel force sensor in standard CMOS with low-cost post-fabrication is developed, which could be integrated into a prosthetic hand or glove. Force and vibration at finger tips can be modulated in real-time to stimulation in different brain areas. The system fully functions in bench testing and *in-vivo* experiments as expected. Based on the preliminary results, the proposed system provides a promising solution in developing fully implantable devices for chronic sensation restoration.

REFERENCES

- [1] J. C. Rothwell, *et al*, "Manual motor performance in a deafferented man," *Brain*, vol. 105, pp. 515-42, Sep 1982.
- [2] S. J. Bensmaia, *et al*, "Restoring sensorimotor function through intracortical interfaces: progress and looming challenges," *Nat Rev Neurosci*, vol. 15, pp. 313-25, May 2014.
- [3] A.G. Richardson, *et al*, "A chronic neural interface to the macaque dorsal column nuclei," *J. Neurophysiol.*, 2016.
- [4] Q. Fan, *et al*, "A 1.8 uW 60 nV/rtHz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes," *JSSC*, vol. 46, no. 7, pp. 1534-1543, 2011.
- [5] H. Zhu, *et al*, "Design of a low power impulse-radio ultra-wide band wireless electrogoniometer," *ISCAS*, 2015.
- [6] X. Liu, *et al*, "A Fully Integrated Wireless Compressed Sensing Neural Signal Acquisition System for Chronic Recording and Brain Machine Interface," *TBioCAS*, vol. 10, no. 4, 2016.